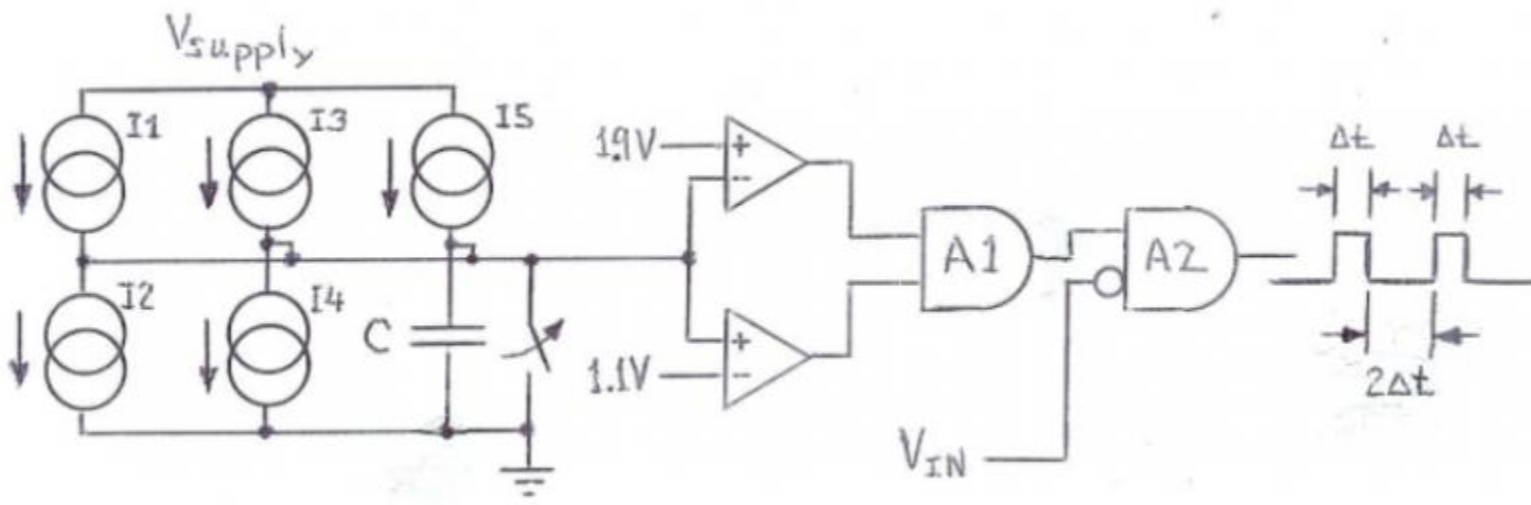
Circuit Challenge 8

The Interview

An electronics design & manufacturing company has invited you in for an interview. You are appearing before a panel of engineers at that company, and they have provided you with the schematic shown below.



The panel explains that this asynchronous circuit is "at rest" most of the time, as follows:

- The switch is closed
- All five current sources are "off", conducting 0µA
- V_{supply} is "always on"
- The 1.1V and 1.9V comparator references are always present
- The comparators and logic gates are always powered up
- C=10µF

The panel then explains that the following sequence of events occasionally occurs:

- The switch opens at a time arbitrarily defined to be t=0
- I1 steps from 0µA to 10µA at t=1 second
- I2 steps from 0µA to 20µA at t=2 seconds
- I3 steps from 0µA to 20µA at t=3 seconds
- I4 steps from 0µA to 20µA at t=4 seconds
- I5 steps from 0µA to 20µA at t=5 seconds

The circuit must output a double pulse with the following properties:

- The output pulses are equal in width (Δt)
- The output pulses are separated by 2Δt

"The entire network will be reset to initial conditions shortly after the double-pulse is detected," the panel explains. "However, the entire system will shut down, and alarms will sound, if the double-pulse is not detected."

The panel then states that you are responsible for V_{IN}. You have available to you a pulse generator that can be triggered from any point in the circuit. It has a programmable delay. It has a programmable pulse width. The pulse generator is limited, however**:** Once triggered, and following the delay, it will deliver only one pulse. Finally, you are told not to be concerned about current, voltage, and capacitance tolerances. "Assume everything is perfect, and assume the current sources are ideal," states one of the panelists.

What You Must Do

1. Tell the panel what signal you will use to trigger the pulse generator.
2. Tell the panel what voltage level will be used for the trigger threshold.
3. Tell the panel how much delay you will program into the pulse generator.
4. Tell the panel how wide the single pulse must be.
5. Draw a waveform showing the current into and out of the capacitor.
6. Draw a waveform illustrating the voltage changes on the capacitor.
7. Draw an output waveform synchronized with 5 & 6 above.

Interested in seeing what will satisfy the interviewing panel? Scroll down.

Analysis for Challenge 8

You will trigger from the positive-going output of A1.

The trigger will occur at 6.1 seconds

The delay will be 0.2 seconds

The pulse width will be 0.4 seconds

And what does the voltage waveform look like on the capacitor? It is the integral of the current into and out of the capacitor, as follows: