Circuit Challenge 9

Many years ago someone (whose name is now lost to antiquity) determined that the circuit concept in **Figure 1** could be used as a basic Digital-to-Analog Converter (DAC). This DAC could, in turn, be embedded in a larger network and become an integral part of an Analog-to-Digital Converter (ADC). If the capacitors were well-matched, if they had all been discharged, and if all the generators had been idling at 0V, then a step voltage on MSB (0V –> V_{REF}) would result in a step voltage at V_{OUT} (0V –> $V_{REF}/2$). In fact, if the generators were sequenced as a binary counter (0000 0000 –> 1111 1111) the output would display as a staircase. With a well-controlled logic sequence, some comparator circuitry, a switch array, a stable voltage reference, and a register to latch the results, this circuit could be placed in a loop, and V_{OUT} could be forced to "window in" on any arbitrary unknown voltage whose value lay reasonably in a range of 0V to V_{REF}. A latched digital word would then represent $V_{Unknown}$. A microprocessor would then evaluate that digital word.

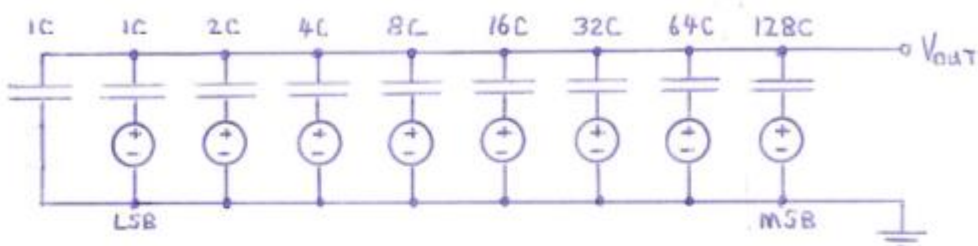


Figure 1

An analysis of the logic, the comparator circuitry, the voltage reference, etc. is not an object of this challenge. We are here interested only in the capacitor array. For those who want to "dive deep" into the particulars of A-to-D structures, take heart: This writeup will provide appropriate references in the online literature. The assumption: If you have made it this far in the challenges you have more than a casual interest in analog circuit theory.

Moving On

You want to integrate (on an IC) the capacitor array. Two problems come to mind:

1. Matching 128C to 1C could be a problem, especially if the 128C is *one* structure. If you argue that you could build the 128C with 128 1Cs, you will then be confronted with a stray capacitance problem related to interconnections.

2. Even if you *could* match the 128C to the 1C, the next issue you confront will be total size. Whatever the *unit* C might be, the *total* capacitance will be 256C.

Someone proposed the solution of **Figure 2**. It was suggested that if C_X is properly sized that V_{OUT} from **Figure 2** will *perfectly* overlay V_{OUT} from **Figure 1**, for the *entire* staircase. If this is true (and you hope it's true), then the matching & sizing problems will be first-order obviated. But is it true?

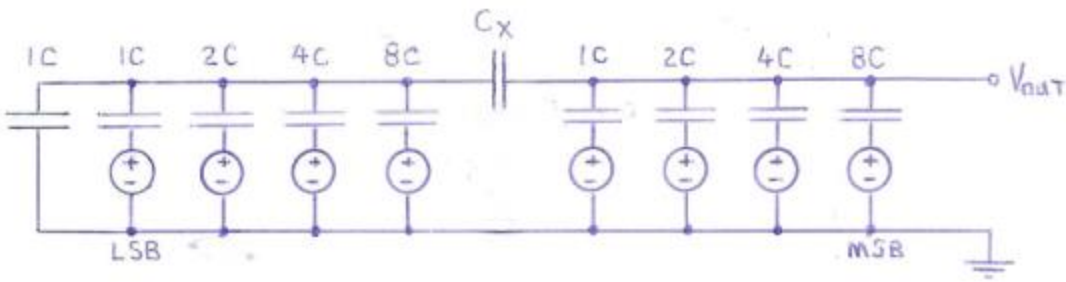


Figure 2

The Challenge

You are to derive the value of C_X. When you think you have it, scroll down.

Analysis for Challenge 9

The derivation of C_X proceeds as follows: We first ask, for **Figure 1**, what total capacitance is "seen" looking to the left of 16C (MSB-3)? The answer is 16C. For equivalency in **Figure 2**, the total capacitance looking into (and from the right of) C_X must be 1C. C_X is in series with 16C, so we can write

$$1/C_X + 1/16C = 1/1C$$

$$1/C_X = 1/1C - 1/16C$$

$$1/C_X = (16/16 - 1/16)/C$$

$$1/C_X = 15/16C$$

$$C_X = (16/15)C$$

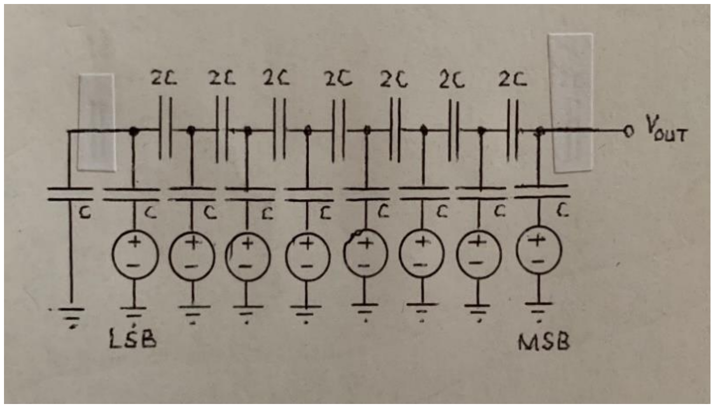
which is precisely the value used by **Culurciello** and **Andreou** (see Figure 2, p. 859, at https://e-lab.github.io/data/papers/TCASIIadc06.pdf). Also, please notice that the total required C is nearly a factor of 8 less when compared with the Σ=256C version.

Another Reference

For another tutorial, start your reading on page 459 of the **M68HC11 Reference Manual**. You will notice (Figure 12-3, p. 471) that C_X has taken on a slightly different value than what was derived in this circuit challenge. This is because of the introduction of a half-unit-value (C/2) capacitor. The use of C/2 is optional; the write-up (beginning on page 467) explains the reason for including it. The derivation of C_X proceeds in the same manner as above, and will (when C/2 is introduced) yield C_X=1.1C.

Is There a Limit to the Number of Bridge Capacitors?

Actually, there can be a bridge capacitor placed between each "bit". The result is a C-2C ladder (analogous to the R-2R ladder). This writer has determined the circuit would look like the figure below (without the switches, comparator circuitry, etc.).



This gives a total of 23C. And what's especially attractive about it is that each 2C bridge capacitor can be constructed from two 1C capacitors. Thus all capacitors may be identically sized (perfect for matching in an integrated circuit environment). Whether or not this topology can be used in an integrated circuit, however, is a strong function of parasitics. Assuming a process is well-modeled, a would-be user of the C-2C ladder would be well advised to put together a rigorous simulation matrix before committing resources to a mask set.

But, as is the case with many good ideas, someone else thought of it first. A couple of references:

- US Patent Number 4,028,694

- https://corescholar.libraries.wright.edu/cgi/viewcontent.cgi?article=3253&context=etd_all
(see Figure 10, page 24, and note that this configuration is for a 10-bit DAC, so there are nine 2C capacitors)